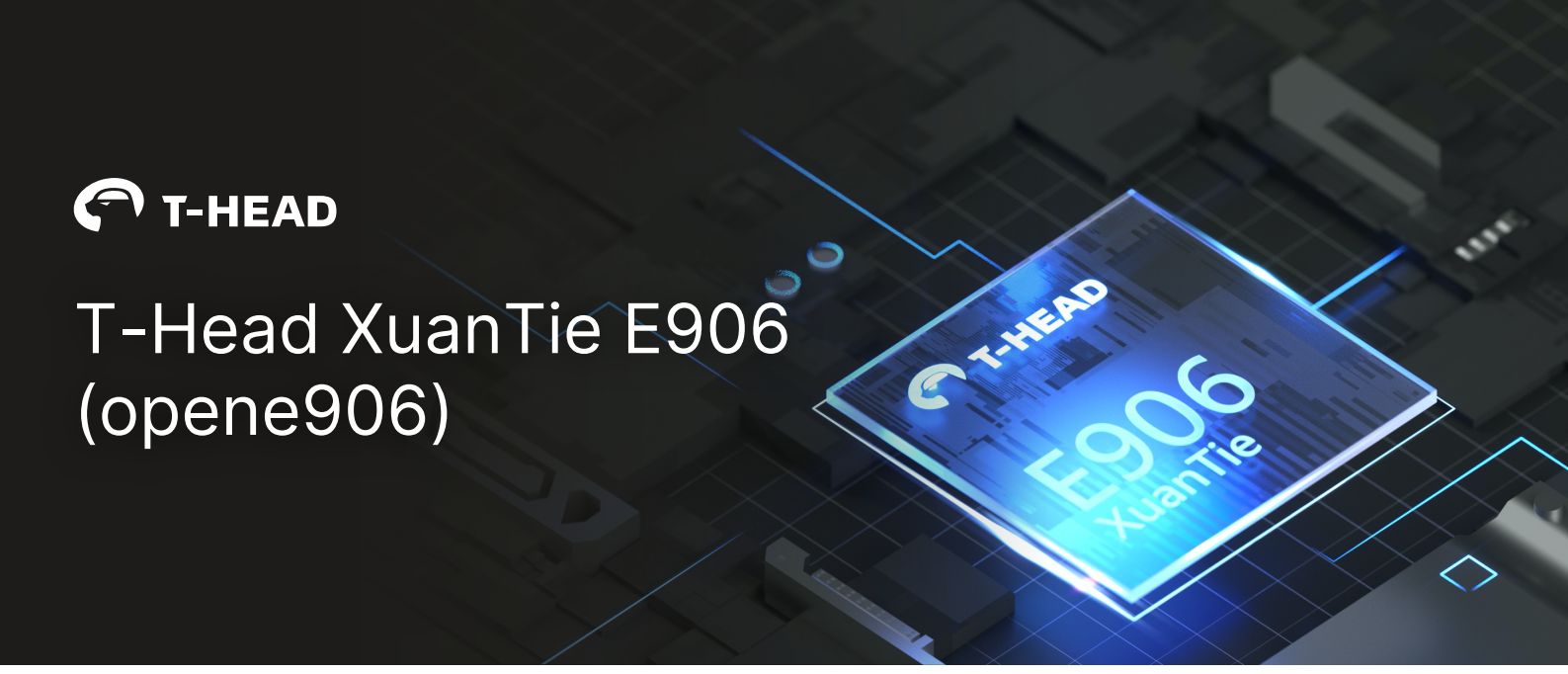
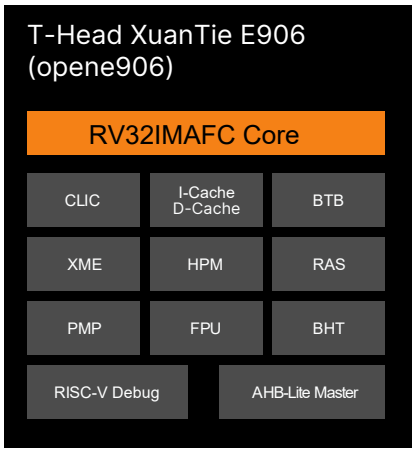
T-HEAD

T-Head XuanTie E906 (opene906)



Overview

The T-Head XuanTie E906 (opene906) is a fully synthesizable, middle-end, microcontroller-class processor that is compatible to the RISC-V RV32IMAFC ISA. It delivers considerable integer and enhanced, energy-efficient floating-point compute performance and fast interrupt response.



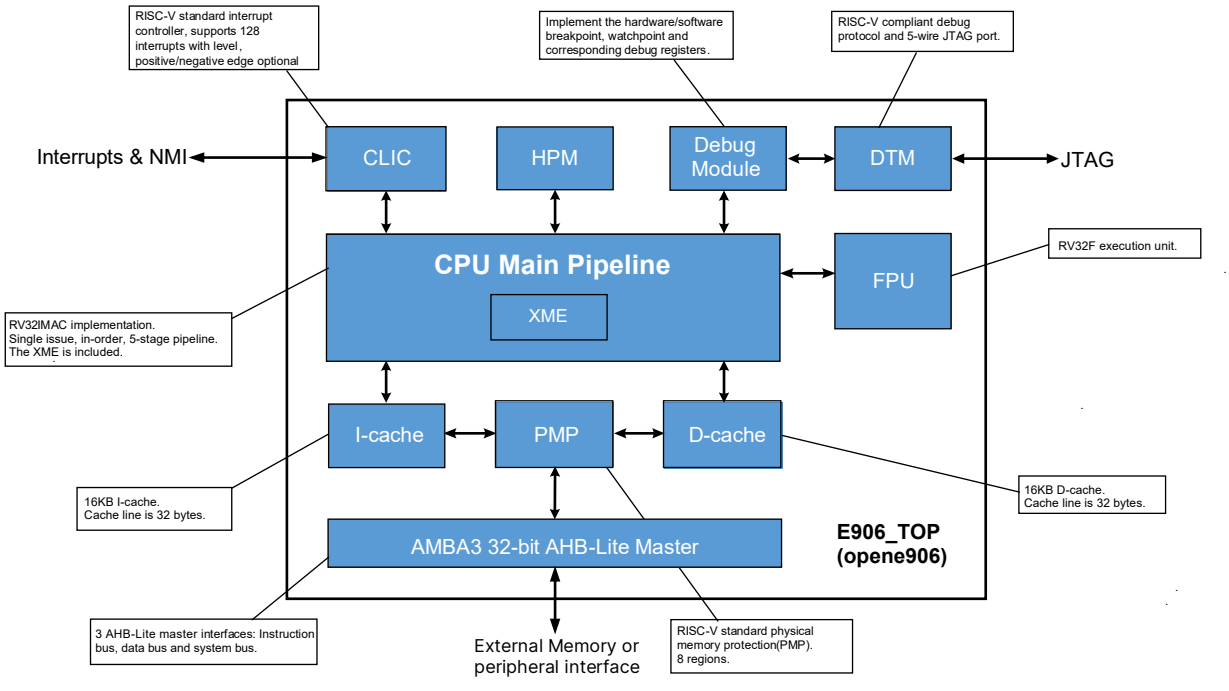
Features

Feature	Description
Architecture	RV32IMAFC
Pipeline	5-stages (integer)
Bus interface	AMBA3 AHB-Lite 32-bit master
FPU	Single precision floating point
Branch Prediction	BHT/BTB/RAS
Instruction cache	16KB
Data cache	16KB
Interrupts	128 interrupts + Non-maskable interrupt (NMI)
Hardware Performance Monitor (HPM)	HPM for performance profiling
Sleep modes	Sleep and deep sleep modes
Debug	RISC-V Debug
XuanTie Extensions	Interrupt accelerating technology Enhanced ISA

XuanTie E906 Components

Processor Overview

The E906 processor adopts a 16/32 bits mixed instruction set and implements a classic 5-stage pipeline for integer. It also supports a single-precision FPU. The processor offers high floating-point compute performance, enhanced ISA extensions, extended fast interrupt handling.



Floating Point Unit (FPU)

Oriented towards the motor and navigation domain, the E906 processor implements a powerful FPU to accelerate the algorithm. The FPU has the following features:

- ◇ Compliant to the RISC-V RV32F;
- ◇ Compliant to the IEEE-754 protocol spec;

Memory Subsystem

E906 has implemented both I-cache and D-cache. They have the following features:

- ◇ 16KB I-cache and 16KB D-cache;
- ◇ 2-way set-associative and the cache line is 32Bytes;
- ◇ FIFO cache replacement policy;
- ◇ Support software invalid and clear (only D-cache) operations through extended instructions;

Physical Memory Protection (PMP)

The E906 processor has implemented the RISC-V PMP which allows machine and user privilege modes to access different address ranges. Only the machine mode has the authority to define the memory access permissions. The PMP has the following features:

- ◇ 8 regions;
- ◇ Read/Write/Execution memory protection;
- ◇ Minimum 128B address range.

Core Local Interrupt Controller (CLIC)

The E906 processor implements the RISC-V standard interrupt controller,CLIC and the CLINT. The CLIC has following features:

- ◇ 128 external interrupts;
- ◇ 8 priority settings;
- ◇ Support level or positive/negative edge interrupt types;
- ◇ Support hardware vector interrupt;
- ◇ The control registers are memory mapped.

Debug Components

The E906 processor adopts RISC-V v0.13.2 version debug spec with standard JTAG to communicate the host and E906 debug unit. E906 has done a lot of optimizations on the debugger and probe and has achieved 800-900KB/s download speed, 4 times faster than the common solutions in the market.
The debug unit supports the following operations:

- ◇ Support hardware/software breakpoints;
- ◇ Support variety trigger settings;
- ◇ Check and modify CPU register resource
- ◇ Single step or multi step flexibly supported.

Hardware Performance Monitor (HPM)

The E906 processor implements optional RISC-V standard HPM to enable software developers to profile the performance. The HPM has following features:

- ◇ Support the ratio of branch prediction profiling;
- ◇ Support the cache miss ratio profiling;
- ◇ Support the execution number of instructions and CPU cycles profiling;
- ◇ Support profiling under machine and user mode;

Interfaces

The E906 has three 32-bit AMBA3 AHB-Lite master buses to communicate with the external memory or peripheral IP which are instruction, data and system bus. The internal requests can be allocated to either bus according to the address. The instruction and data buses can only be connected to the memory other than the peripheral IPs.

XuanTie MCU Enhanced Extensions (XME)

The E906 processor implements the XME to deliver more powerful features such as:

- ◇ Support fast interrupt handling and the response time is 18 CPU cycles;
- ◇ Support tail-chain for both vector and non-vector interrupts;
- ◇ Support NMI;
- ◇ Support Lockup;
- ◇ Support sleep and deep sleep;
- ◇ Support soft reset operation;
- ◇ Support configurable reset address through top port during integration;

Software Ecosystems

- ◇ Optimized compiler, assembler, linker and binary tools are contributed to GNU and supported officially;
- ◇ Enhanced ISA is supported by GCC and LLVM;
- ◇ QEMU is contributed and supported officially;
- ◇ Code size optimized runtime lib;
- ◇ Supply Keil-like Integrated Development Environment (CDK);
- ◇ Support mainline IDE and debug probe such as IAR IDE, OpenOCD, Lauterbach debugger, Segger J-Link;
- ◇ Support FreeRTOS, uCos, RT-Thread and AliOS-Things.

Configuration Options

Feature	Options
Architecture	RV32IMAFC
Instruction cache	16KB
Data cache	16KB
Branch History Table	8Kb
Branch Target Buffer	Present
Interrupts	128
PMP	8 regions
HPM	RISC-V standard HPM